**Philadelphia University**

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**Faculty of Information Technology**

**Department of CS**

**Examination Paper**

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**Computer Organization and Design** **750233** Section :- **1 First Exam**

**2nd Semester of academic year 2016/2017 Date**: Dec, 24, 2016  **Time**: 50 minutes

**Information for Candidates**

1. *This examination paper contains Six questions, totaling*  ***40*** *marks. (divided by 2 to become out of 20)*
2. *The marks for parts of questions are shown in round brackets.*

## Advice to Candidates

 *1. You should attempt all questions.*  *2. You should write your answers clearly.*

**Part I:**

***Objectives****:* ***Objectives****: The aim of the question in this part is to evaluate your required minimal knowledge about the* Computer Organization and Design *in general.*

**Question 1: Choose the most appropriate answer of the following: (8 M, 1 M each)**

1. Represent the following decimal number in BCD-code: (674)10 = (?)BCD.

a) (011001110100) BCD b) (010101010101)BCD  c) (011001110101)BCD d) (011001110011)BCD

1. Choose the right result of the following conversion: (F3C)16 = (?)8.

a) (7373)8 b) (8383)8  c) (8484)8 d) (7474)8

1. By simplifying the following expression F = (A + B)'(A' + B')', choose the right result:

a) F = A'B' b) F = 1 c) F = 0 d) F = A' + B'

1. The following Sum of Minterms F (A, B, C) = ∑(1, 3, 5, 7) should be represented by:

a) F (A, B, C) = A'B'C' + A'BC' + AB'C + ABC' b) F (A, B, C) = A'B'C + A'BC + AB'C + ABC

c) F (A, B, C) = A'B'C + AB'C' + ABC' + ABC d) F (A, B, C) = A'B'C' + A'B'C + AB'C' + ABC

1. Which of the following is a sequential circuit:

a) Full-Adder b) D flip-flop c) Decoder d) Multiplexer

1. A combinational circuit has three inputs A, B, C,where Cis the least significant bit and Ais the most significant

 bit. The output from the circuit is 1 when the binary value of the input is less than 3; otherwise, the output is 0.

 Which of the following expressions represents the output from this circuit?

a) A'(B' + C') b) AB + AC c) A (B + C') d) A'B + AC'

1. Which of the following is considered a correct function for a 3-bit parity generator and 4-bit parity checker using an odd-parity bit?
2. P = x ⊕ y ⊗ z, Error= x ⊕ y ⊗ z ⊗ P b) P = x ⊕ y , Error= x ⊗ y ⊗ z ⊗ P

c) P = x ⊕ y ⊕ z, Error= x ⊕ y ⊕ z ⊕ P d) None of them. Specify (\_\_\_\_\_\_\_\_\_\_)

1. The equivalence to the dual of (x y ' + xyz ' + x ' z) is:

a) *x'y + x'y' z+ x z '* b) (*x'+y) ( x ' + y'+z) (x + z ')*

c) (*x + y' ) ( x + y + z' ) (x' + z* ) d) *None of the above Specify: (\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ )*

***Question 2: (4 Marks)***

Using truth table prove the validity of De Morgan's theorem for the following function after finding the result at the right side of the function.

 (A**'** + AB**'** (AD**'** + B**'** C ) . A**'** C **'** )**' = ?**

***Question 3: (5Marks)***

Simplify the following Boolean function in Product-of-Sums form by means of a four-variables map. Draw the logic diagram with 1) OR – AND gates, 2) NOR gates.

F(w, x, y, z ) = ∑ (2, 3, 4, 5, 6, 7, 11, 14, 15)

 ***F = (w' + y) ( x + y ) ( w' + x + z )***

**Question 4*: (6Marks)***

The following transfer statements specify a memory. Explain the memory operation in each case.

1. xT3: R2 M[AR], AR PC
2. xT3: M[AR] AR, AR DRPC . Assume the value of PC is (56) and DR is (32), explain the memory operation and what is the written value in memory?
3. R5 M[R5]

***Question 5: ( 6 Marks)***

Perform the arithmetic operations (+72) + (- 85) and (+72) + (+ 85) with binary numbers in signed 2's complement representation. Use eight bits to accommodate each number together with its sign. Show the overflow occurs in both cases.

**Part II Familiar Problem Solving:**

***Objective****: The aim of the question in this part is to evaluate your required knowledge for solving problems in computer data representation.*

***Question 6: ( 5 Marks)***

Represent the number (+46.5)10 as a floating-point binary number with 24-bits. The normalized fraction mantissa has 16 bits and the exponent has 8 bits.

**Part II: Unfamiliar Problem Solving:**

***Objectives****:* ***Objectives****: The aim of the question in this part is to evaluate your required knowledge about the computer organization.*

***Question 7: (6 Marks)***

Derive the circuits for a 3 –bits parity generator and 4- bit parity checker using an even-parity bits.